CLAIMS:

1. A display method comprising

generating (1) images comprising source data (SDA) and source frame synchronization instants (SSI) having a source frame rate (SFR),

storing (2) the source data (SDA) in a frame memory (5) under control of a first address pointer (AP1) having a start address (DSA) being determined by the source frame synchronization instants (SSI),

reading (2), during a read period (RP), display data (DDA) from the memory (5) under control of a second address pointer (AP2) having a start address (SSA) being determined by display frame synchronization instants (DSI) having a display frame rate (DFR),

displaying (3) the display data (DDA) on a matrix display (4), and

controlling (2) the source frame rate (SFR) or the display frame rate (DFR) to obtain, in a stable situation, the first address pointer (AP1) and the second address pointer (AP2) starting with an offset in time (TO) which has a fixed polarity during the read period (RP).

2. A display system comprising

a video source (1) for generating images comprising source data (SDA) and source frame synchronization instants (SSI) having a source frame rate (SFR),

means for storing (2) the source data (SDA) in a frame memory (5) under control of a first address pointer (AP1) having a start address (DSA) being determined by the source frame synchronization instants (SSI),

means for reading (2), during a read period (RP), display data (DDA) from the memory (5) under control of a second address pointer (AP2) having a start address (SSA) being determined by display frame synchronization instants (DSI) having a display frame rate (DFR),

means for displaying (3) the display data (DDA) on a matrix display (4), and

means for controlling (2) the source frame rate (SFR) or the display frame rate (DFR) to obtain, in a stable situation, the first address pointer (AP1) and the second address

pointer (AP2) starting with an offset in time (TO) which has a fixed polarity during the read period (RP).

3. A display system as claimed in claim 2, wherein the means for controlling (2) comprise:

means for comparing (33) the source frame synchronization instants (SSI) and the display synchronization instants (DSI) or signals related thereto, and

means for adapting (33) the source frame rate (SFR) or the display frame rate (DFR) in response to the comparing (33) to obtain the second pointer (AP2) always lagging the first pointer (AP1) during the read period in time (RP), or the other way around.

4. A display system claimed in claim 2, wherein the means for controlling (2) comprise:

means for determining (33) the offset in time (TO) between one of the source frame synchronization instants (SSI) and one of the display frame synchronization instants (DSI) succeeding each other, and

means for adapting (33) the source frame rate (SFR) or the display frame rate (DFR) to obtain a substantially identical source frame rate (SFR) and display frame rate (DFR), and a predetermined fixed value of the offset in time (TO).

5. A display system as claimed in claim 4, wherein the means for adapting (33) are arranged to obtain the offset in time (TO) between the first pointer (AP1) and the second pointer (AP2) being substantially equal to half a source write period (WP), the source write period (WP) being the period in time required for the storing (2) of the source data (SDA) of one source frame of the source data (SDA).

6. A display system as claimed in claim 2, wherein the means for displaying (3) the display data (DDA) further comprise:

means for generating (322) a clock signal (CLK), and

means for generating (320) the display frame synchronization instants (DSI) using the clock signal (CLK), and wherein

the means for controlling (2) the display frame rate (DFR) comprise means for adapting (32) a frequency of the clock signal (CLK).

7. A display system as claimed in claim 2, wherein the means for displaying (3) the display data (DDA) further comprise:

means for generating (322) a clock signal (CLK),

means for generating (321) line instants (LI) indicating a start of the lines of the display data (DDA) using the clock signal (CLK), the line instants (LI) determining line periods (TL), and

means for generating (320) the display frame synchronization instants (DSI) using the line instants (LI), and wherein

the means for controlling (2) the display frame rate (DFR) comprise means for adapting (32) a frequency of the clock signal (CLK) to vary a duration of the line periods (TL).

8. A display system as claimed in claim 2, wherein the means for displaying (3) the display data (DDA) further comprise:

means for generating (322) a clock signal (CLK),

means for generating (321) line instants (LI) indicating a start of the lines of the display data (DDA) by counting the clock signal (CLK), the line instants (LI) determining line periods (TL), and

means for generating (320) the display frame synchronization instants (DSI) using the line instants (LI), and wherein

the means for controlling (2) the display frame rate (DFR) comprise means for adapting (32) the line periods (TL) by varying a number of clock pulses of the clock signal (CLK) to be counted.

9. A display system method as claimed in claim 2, wherein a display frame period (DFP) has a duration being an inverse of the display frame rate (DFR) and comprises the means for read period (RP) and an idle period (ID), wherein during the read period (RP), the means for reading (2) are arranged for reading the display data (DDA) from the memory (5) under control of the second address pointer (AP2), and wherein during the idle period (ID) no display data (DDA) is read from the memory (5), and wherein the means for controlling (2) the display frame rate (DFR) comprises means for varying the idle time (ID).

10. A display system as claimed in claim 2, wherein the means for controlling (2) comprise:

means for determining (33) the offset in time (OT), and

means for adapting (33) the display frame rate (DFR) to obtain a display frame rate (DFR) being substantially identical to two times the source frame rate (SFR) and to obtain a predetermined fixed offset in time (OT), by having

(i) the second pointer (AP2) pointing to a first source video line (1) of an already stored source video frame (F1) at an instant (t13) preceding the instant (t14) the first pointer (AP1) is pointing to a first source video line (1') of a next source video frame (F2) to read the first source video line (1) before the first source video line (1') of the next source video frame (F2) is stored, and

(ii) the second pointer (AP2) pointing to a last source video line (N') of the next source video frame (F2) at an instant (t19) later than an instant (t17) the first pointer (AP1) is pointing to the last source video line (N') of the next source video frame (F2) to read the last source video line (N') of the next source video frame (F2) after it has been stored.

11. A display system as claimed in claim 2, wherein a display frame period (DFP) has a duration being an inverse of the display frame rate (DFR) and comprises the read period (RP) and an idle period (ID), wherein during the read period (RP), the means for reading (2) are arranged for reading the display data (DDA) from the memory (5) under control of the second address pointer (AP2), and wherein during the idle period (ID) no display data (DDA) is read from the memory (5), and wherein the means for controlling (2) comprise:

means for setting (32) a free running display frame rate to a value lower than the value of the source display frame rate (SFR), wherein a duration of the read period (RP) is shorter than a source frame period (SFP), and

means for restarting (32) the display frame periods (DFP) in response to received source synchronization instants (SSI).

12. A display system as claimed in claim 11, further comprising means for adapting (33) the display frame rate (DFR) to become substantially equal to two times the source frame rate (SFR).